

**UNITED STATES DEPARTMENT OF COMMERCE****Patent and Trademark Office**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/466,934 12/20/99 YAMAGUCHI

Y 0057-2567-2Y

□ MMC2/0718  
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EXAMINER

STEVENS, A

ART UNIT	PAPER NUMBER
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2812

DATE MAILED:

07/18/01

Please find below and/or attached an Office communication concerning this application or proceeding.

**Commissioner of Patents and Trademarks**

<b>Office Action Summary</b>	Application No.	Applicant(s)
	09/466,934	YAMAGUCHI ET AL.
	Examiner	Art Unit
	Andre' C Stevenson	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is FINAL.      2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-23 is/are pending in the application.
  - 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-23 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claims \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are objected to by the Examiner.
- 11) The proposed drawing correction filed on \_\_\_\_ is: a) approved b) disapproved.
- 12) The oath or declaration is objected to by the Examiner.

#### Priority under 35 U.S.C. § 119

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

#### Attachment(s)

- 15) Notice of References Cited (PTO-892)
- 16) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 17) Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.
- 18) Interview Summary (PTO-413) Paper No(s) \_\_\_\_.
- 19) Notice of Informal Patent Application (PTO-152)
- 20) Other: \_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 6 and 23 are rejected under 35 U.S.C. 102(e) as being unpatentable over Saito (U.S. Pat. No.6100570).

### **Claim #1**

A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

A plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer (*figure #20, reference 201& 202, column 6 lines 53 through 58*);

At least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other; and

A body region provided in said SOI layer and capable of externally fixing electric potential (*column 8 lines 34 through 42*),

Wherein at least part of said at least one isolation region includes a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof, said semiconductor region serving as part of said SOI layer and being formed in contact with at least one of said plurality of device formation regions and said body region (*column 9 lines 1 through 5*).

**Claim #6**

A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

A plurality of device formation regions in which predetermined devices are to be formed respectively, said plurality of device formation regions being provided in said SOI layer (*figure #20, reference 201& 202, column 6 lines 53 through 58 & figure #7, reference 71, 73& 77, column 9 lines 1 through 5*);

At least one isolation region provided in said SOI layer for insulatively isolating said plurality of device formation regions from each other (*column 2 lines 23 through 31*); and

A body region capable of externally fixing electric potential (*figure #3, reference 36& 39, column 8 lines 34 through 42*)

wherein said body region is formed in contact with one of top and bottom surfaces of at least one of said plurality of device formation regions (Column 7, line 35 through 36).

**Claim # 23**

A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulation layer and an SOI layer, said semiconductor device comprising:

A device formation region in which a predetermined device is to be formed, said device formation region being provided in said SOI layer (*figure #2, reference 21 – 28, column 9 lines 18 through 34*); and

A peripheral isolation region provided in said SOI layer and surrounding said device formation region, said peripheral isolation region including a partial isolation region having a partial isolation region having a partial insulation region formed in an upper part thereof and a semiconductor region formed in a lower part thereof and serving as part of said SOI layer (*column 9 lines 1 through 15*)

Wherein said semiconductor region is formed in contact with said device formation region and is floating (*figure #8, column 11 lines 8 through 11*).

Applicant's arguments filed 5/10/01 have been fully considered but they are not persuasive.

➤ 1) Applicant states "Nothing corresponding to a partial isolation region can be found in any of the figures or text relied upon by the Office Action in Saito, or employed anywhere else in the Saito reference".

- ❖ **Answer:** Saito provides a method for both etching the isolation (insulating) layer of the device at different thickness and provides a method for doping the layer at different levels. Thus, providing a method to create insulation effects at different strengths. Therefore it would have been obvious to one with ordinary skill in the art to vary one or both of the parameters to achieve a partial insulating condition.
- 2) Applicant states "The official action fails to show in the Saito reference "a body region capable of externally fixing electric potential, wherein said body region is formed in contact with one of the top and bottom surfaces of at least one of said plurality of device formation regions."
- ❖ **Answer:** Saito clearly shows in figure #3 item 31, Electric potential wells that formed in order under electrodes 36-39.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The evidence submitted is insufficient to establish a conception of the invention prior to the effective date of the Hembree (U.S. Pat. No.6078186) reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (703) 308 6227. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308 3325. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956.

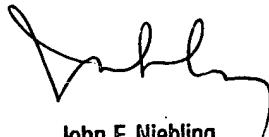
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John F. Niebling  
Supervisory Patent Examiner  
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